

Properties of Magnetic Tunnel Junction bits for MRAM

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Jon Slaughter, ANL/APS Nanomagnetism Workshop, 31August, 2004



Outline

Background

Reading from an array of MTJ bits

- opportunities

Writing bits in an array

- opportunities

Summary

MRAM Attributes

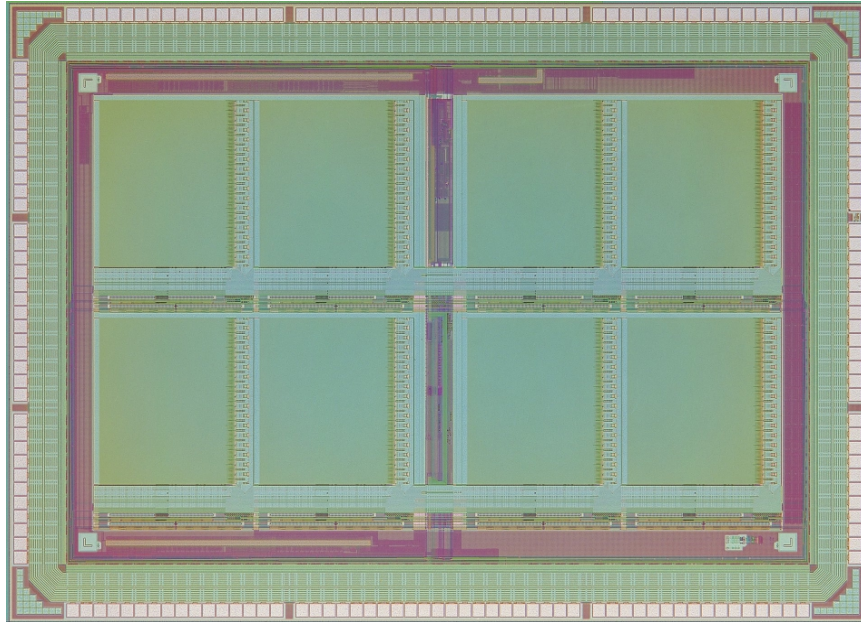
MRAM offers multiple memory capabilities that are currently realized by separate memories: *universal memory*

Non-Volatility with fast programming, no program endurance limitation

Random Access with no refresh.

Non-destructive read

4Mb MRAM Circuit

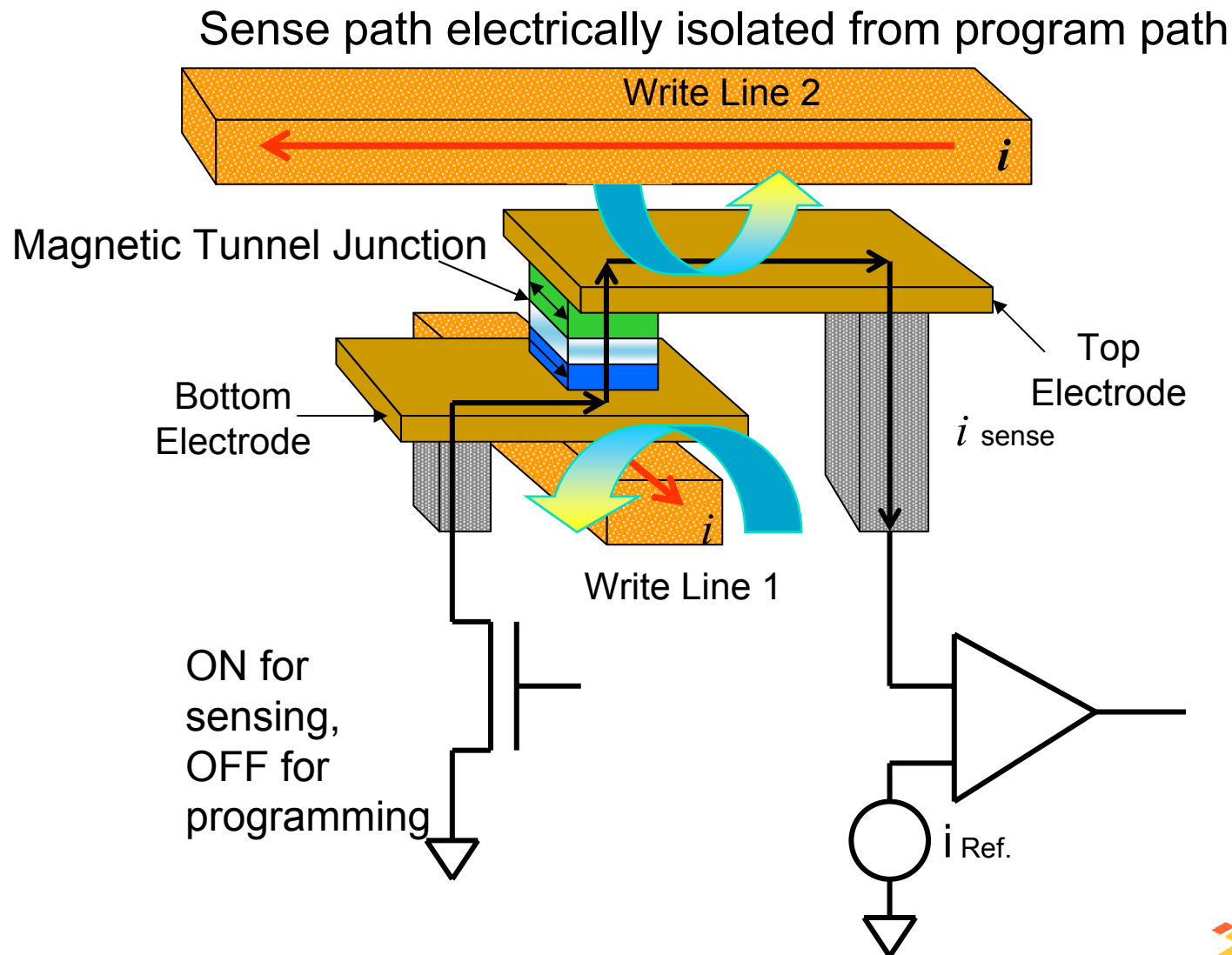


4Mb MRAM die

- 0.18 μm CMOS with 3 layers of Aluminum and 2 layers of Copper Interconnects
- Cladded write lines
- 256K x16 Organization
- 3.3V Supply Voltage
- Symmetrical 25ns read and write timing
- Bit Cell Size = 1.55 μm^2
- Die Size 4.5 x 6.3mm

Proc. IEEE International Electron Devices Meeting 2003
Proc. Intermag 2004, IEEE Trans. Mag., in press.
Proc. ISSCC 2004

4Mb MRAM Bit Cell



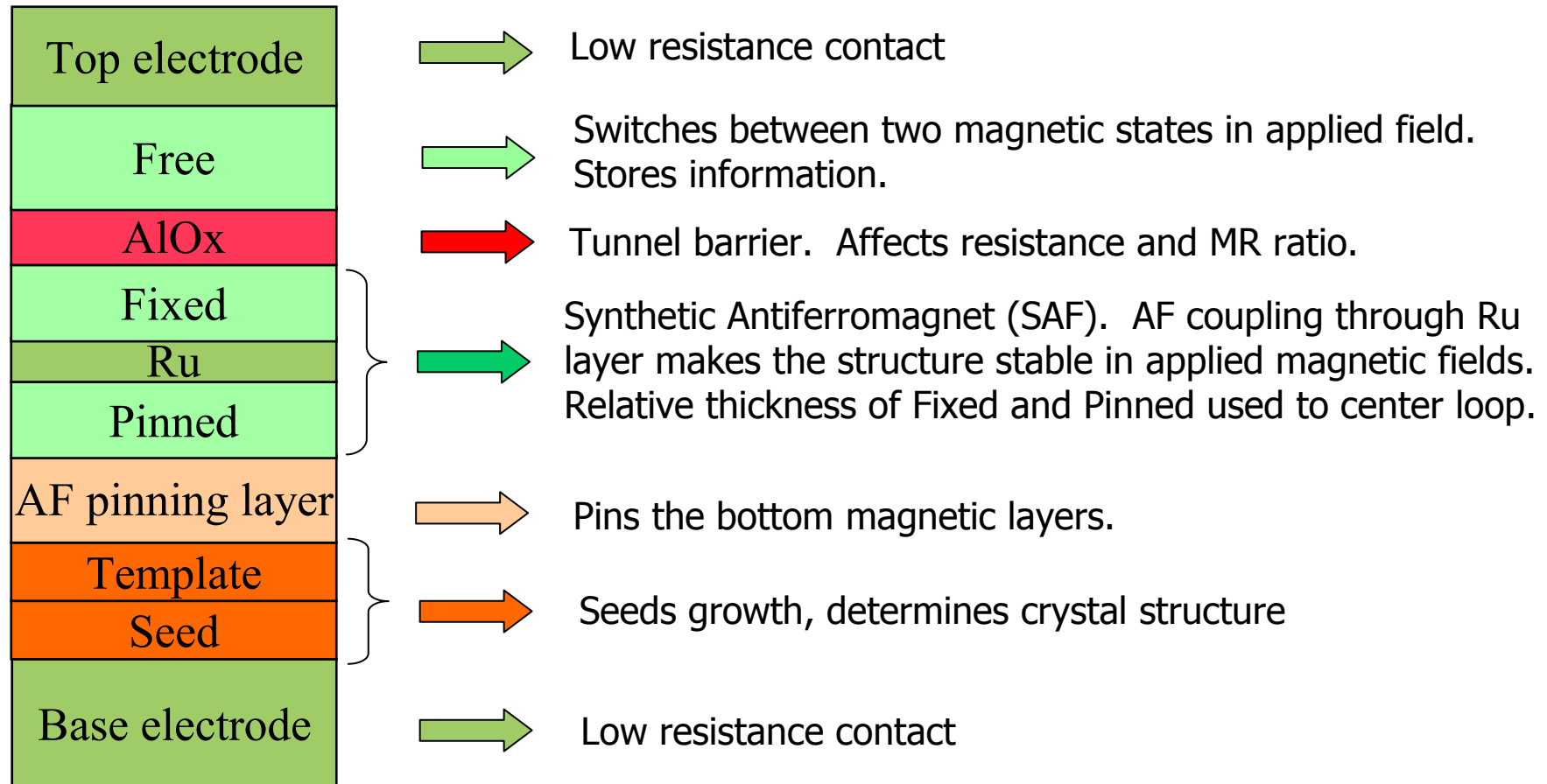
Magnetic Tunnel Junction Material

Jon Slaughter, ANL/APS Nanomagnetism Workshop, 31August, 2004

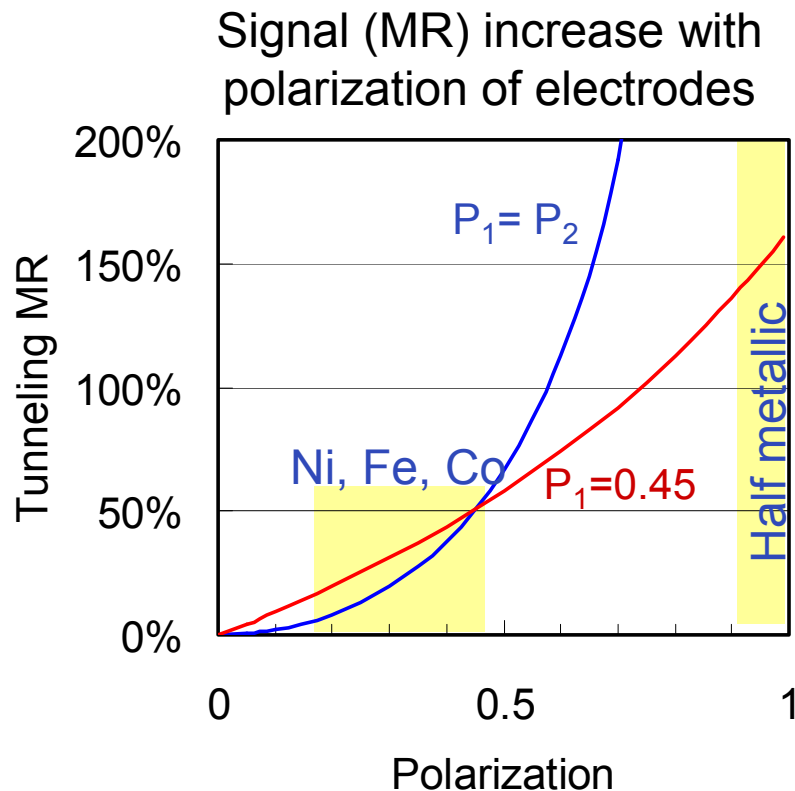


Full MTJ Stack for MRAM

Full MTJ Stack for MRAM



Effect of Increasing Polarization



One half-metallic electrode would give a huge signal boost for MRAM

Recent reports of high TMR with crystalline MgO barrier indicate potential for similar effect.

Increase in signal would

- relax requirements on R distributions
- provide higher speed
- enable alternate architectures

Finding a high-polarization material system that can be applied commercially is a huge challenge and huge opportunity!

Reading from an array

High MR is Not Enough

$$MR = \Delta R / R_{\text{low}}, \Delta R = R_{\text{high}} - R_{\text{low}}$$

$$\text{Signal} = R_{\text{cell}} - R_{\text{ref}}$$

- $\frac{1}{2}$ of ΔR available for sensing

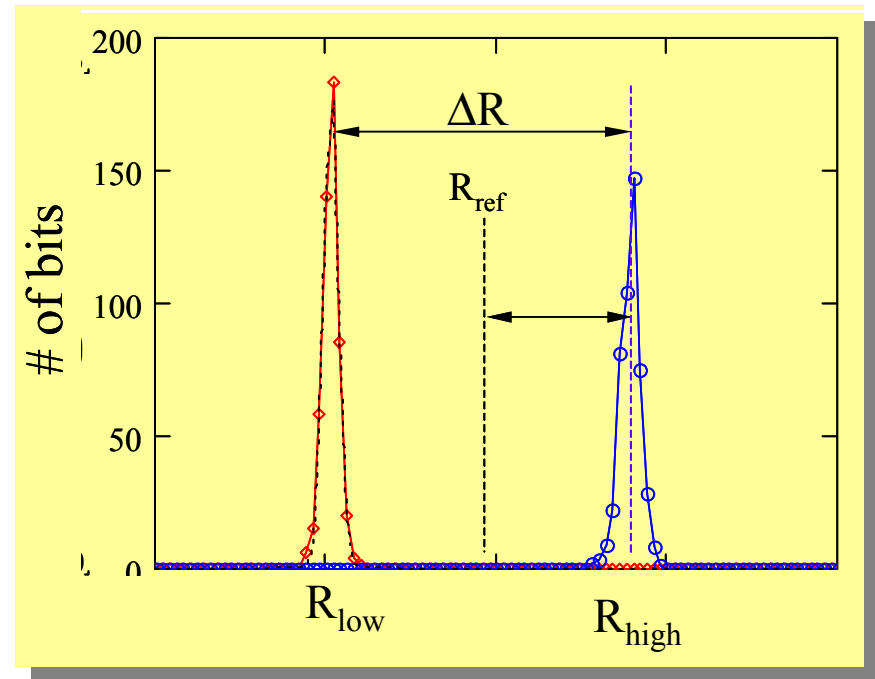
Circuit works at finite bias

- MR is reduced by bias dependence of MR

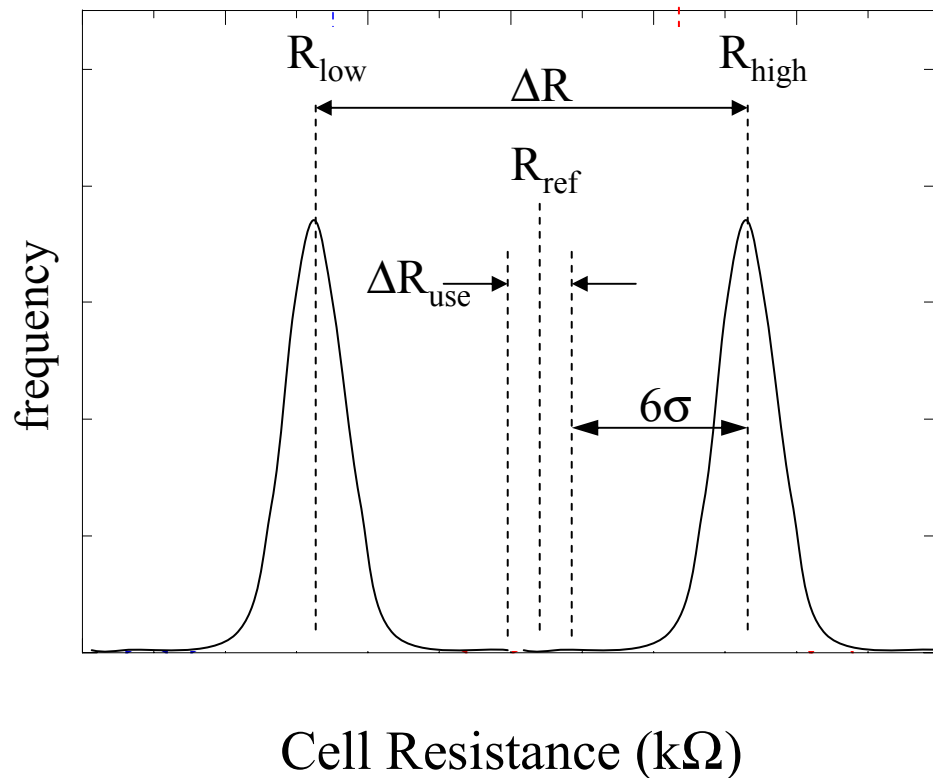
Must sense all bits in the array

- Circuit must work with bits in tails of the R distribution

Array: R_{cell} Histogram



Resistance Variation In Array



Resistance distribution reduces useable MR.

For six-sigma yield in the array, need:
 $\Delta R/2 > 6\sigma$

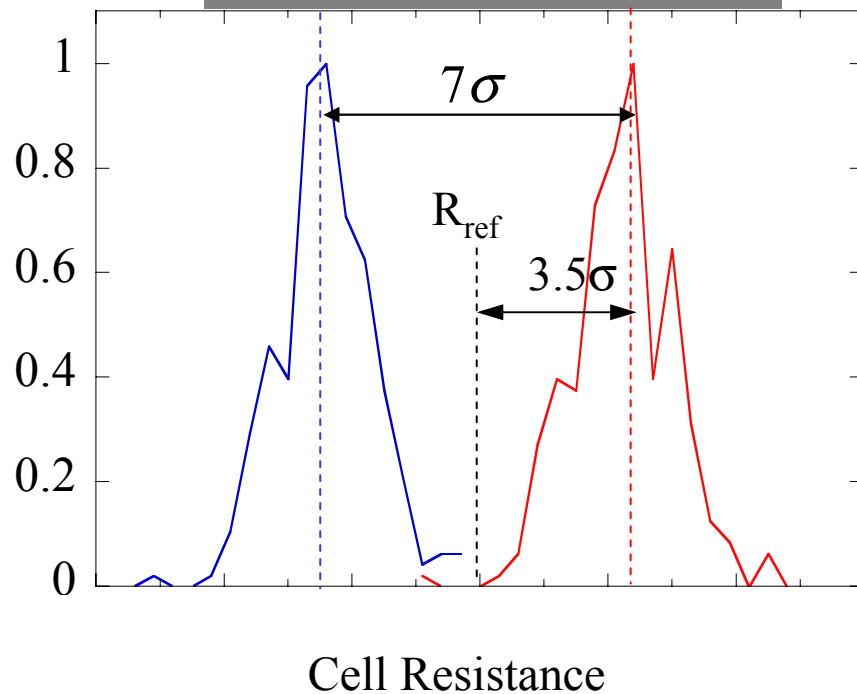
NOT related to wafer-level uniformity

$RA=10.4 \text{ k}\Omega\text{-}\mu\text{m}^2$, $\sigma=6\%$

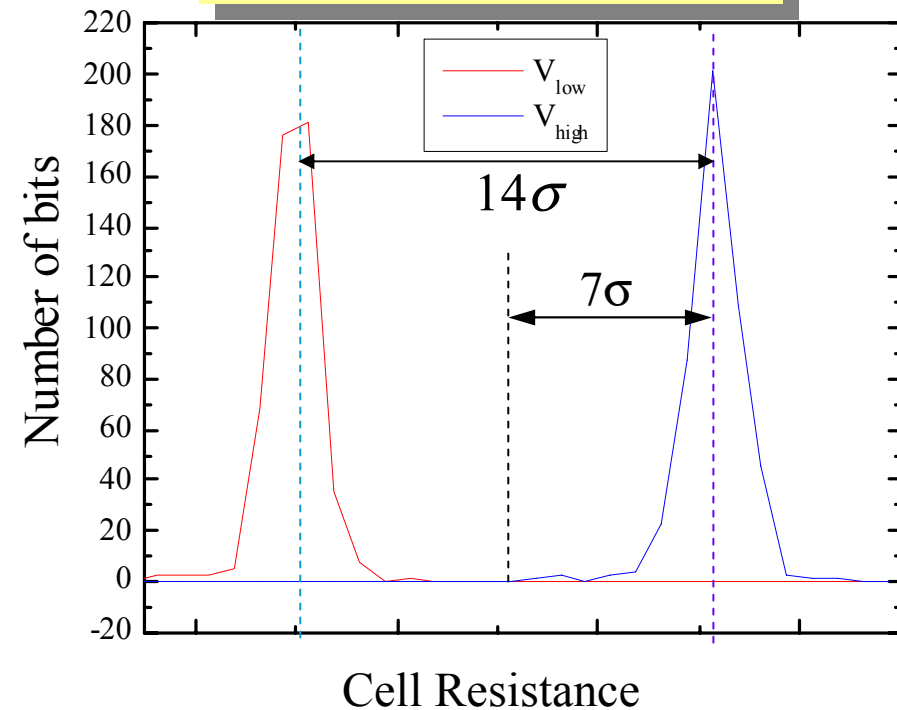
	11.3	11.0	10.5	10.5	10.9	12.3	
11.7	10.3	9.74	9.88	9.65	9.80	10.2	11.5
10.3	9.54	10.9	10.6		10.3	9.74	10.5
10.1	9.68	10.4	10.8	10.8	10.7	9.85	10.7
	9.80	10.9	10.5	10.8	10.5	9.86	10.2
10.3	9.45	10.1	10.4	10.6	9.87	9.62	10.9
	10.2	9.52	9.43	9.56	9.59	10.2	
		11.2	10.2	10.4	11.0		

Resistance Uniformity Within Array

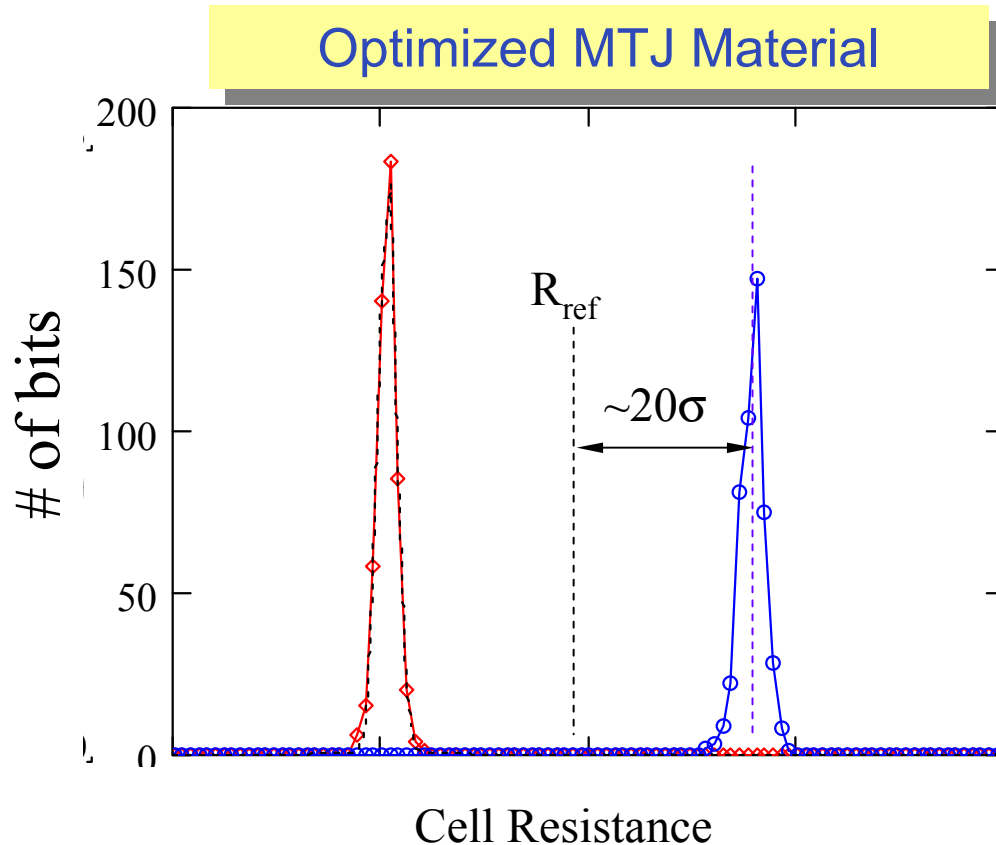
Common MTJ Material



Improved MTJ Material



Resistance Distribution Within Array



High MR and narrow RA distribution:
 $\sim 20\sigma$ margin on read

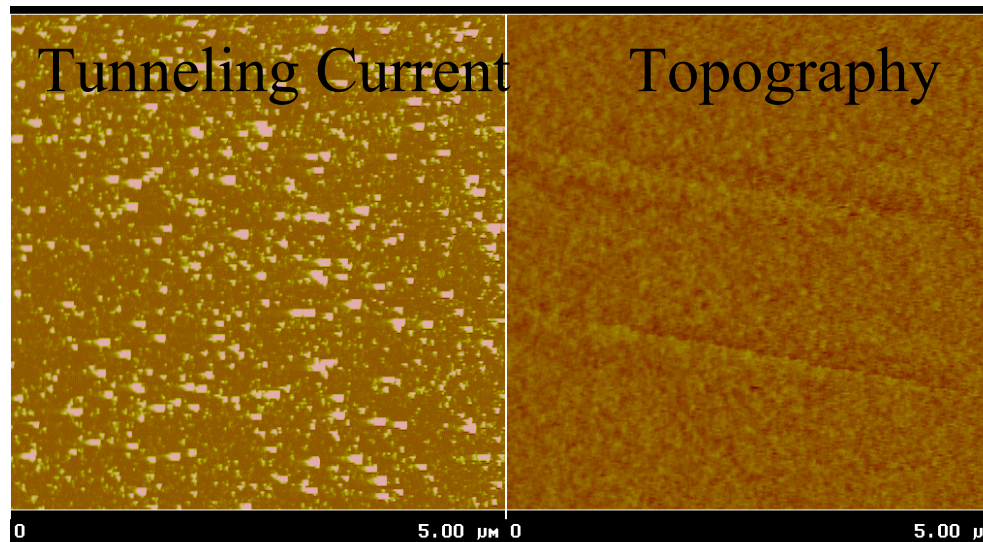
- Distribution width $< 1\%$
- MR(at bias) $\approx 30\%$

Other possible contributors to distribution widths:

- Lithography
- Etching
- Process damage

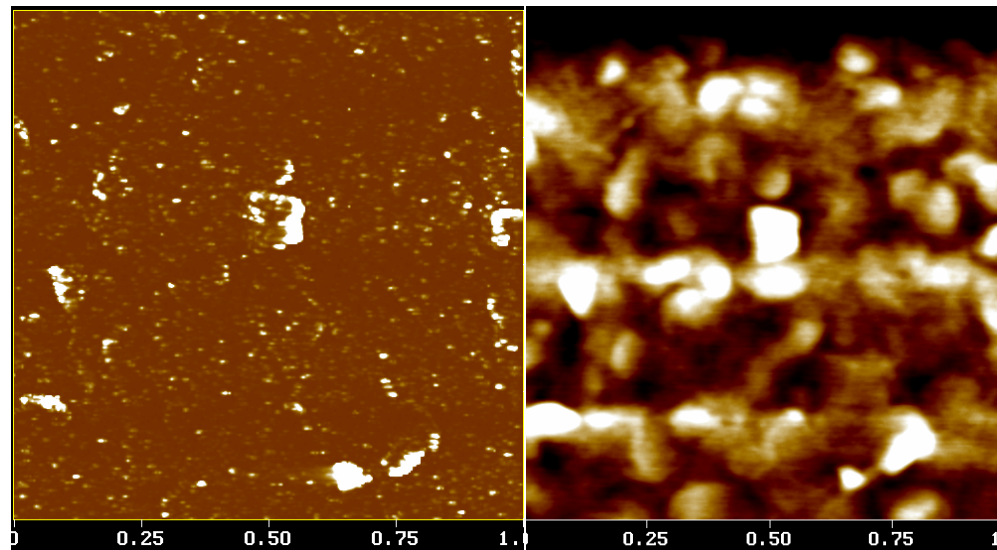
Tunneling AFM Measurements of Barrier Uniformity

smooth



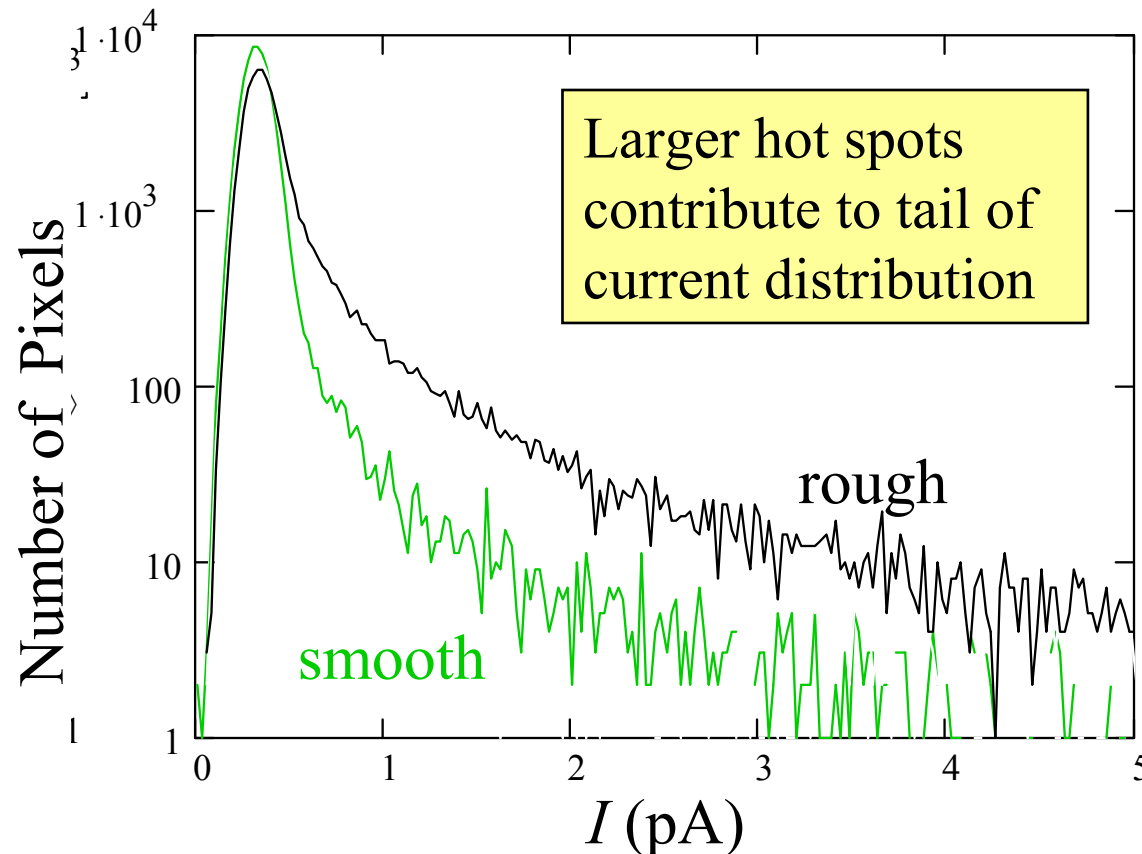
$5\mu\text{m} \times 5\mu\text{m}$

rough



$1\mu\text{m} \times 1\mu\text{m}$

Current histogram: Tunneling AFM



Comparative analysis

- Follows log-normal distribution
- σ is figure of merit
- Control more difficult for lower RA and smaller bits

Research Opportunity:

Insulating material with lower barrier height would allow thicker barriers for low RA material. Many materials requirements to meet.

High MR is Not Enough

High MR materials are valuable if tunnel barrier quality is maintained

- **Figure of merit for read is $\Delta R/\sigma$**
- **Ideal improved material would provide increased MR with same σ**
- **Roughness and interface quality just as important as ‘polarization’**

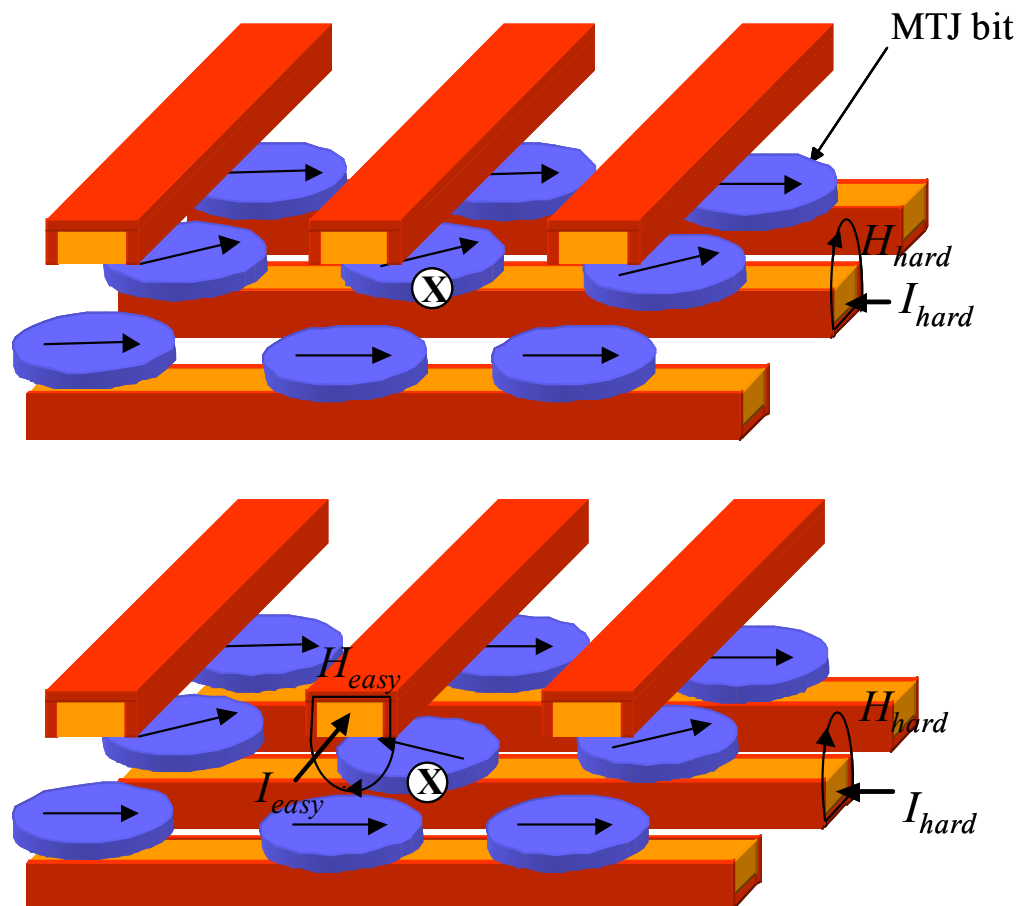
Opportunities in MTJ Material

Improved MR/ σ

- **High polarization materials for the tunneling electrodes**
 - Proof of half-metallicity or high polarization (e.g. is Fe_3O_4 really $\frac{1}{2}$ metallic?)
 - Stability of the interface with tunnel barrier
- **Tunnel barrier materials (e.g. AlOx & MgO)**
 - Growth and interface studies
 - Stability: e.g. migration of atoms under thermal or electrical stress
- **Electrode/barrier combinations**
 - Smoothness of interfaces
 - Control of tunneling hot spots on small scale
 - Practical process for deposition/growth: what materials have the most promise for applications?

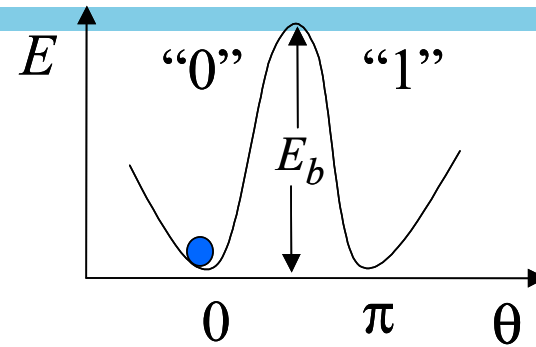
Writing bits in an array

Conventional MRAM: Bit Selection



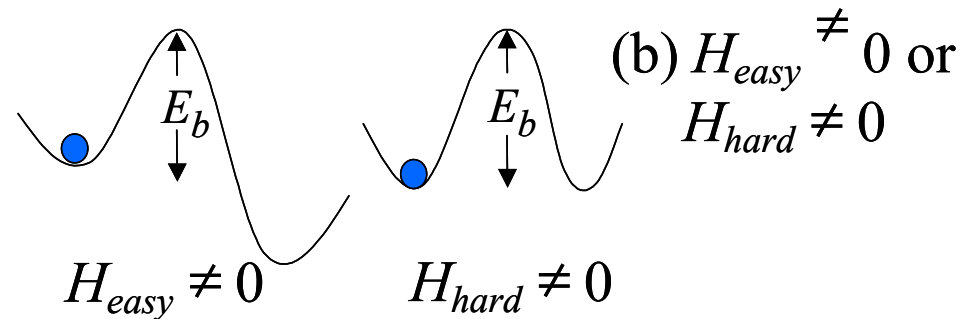
Energy Barrier Model of Magnetization Reversal

Unselected



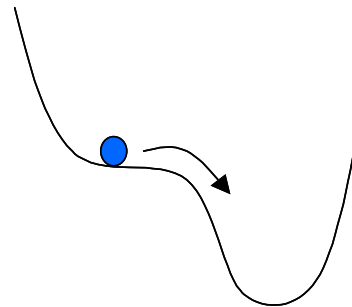
(a) $H = 0$

$\frac{1}{2}$ -Selected
Lower barrier



(b) $H_{easy} \neq 0$ or
 $H_{hard} \neq 0$

Selected



(c) $H_{hard} \neq 0$
and $H_{easy} \neq 0$

New Writing Approach: “Savtchenko Switching”

**Proposed at Motorola by the late
Leonid Savtchenko**

- US Patent 6,545,906

**Write operation is a rotation of a
balanced SAF**

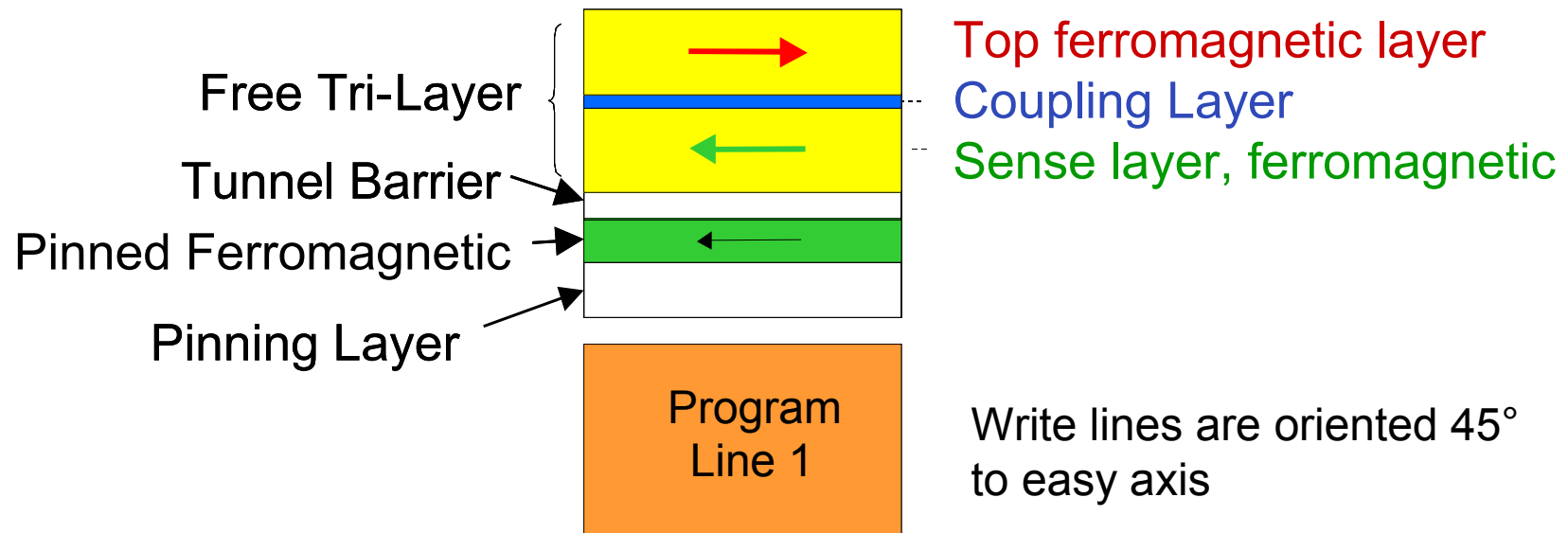
Toggle rather than “forced” write



Leonid Savtchenko

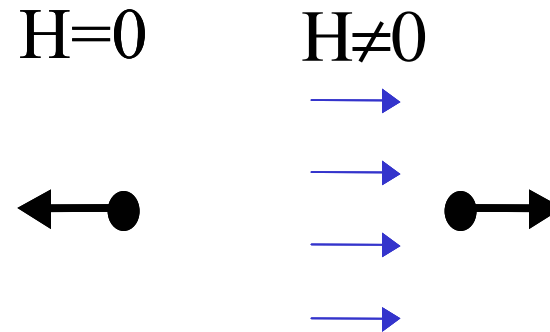
Toggle MRAM Bit Cell

Program Line 2

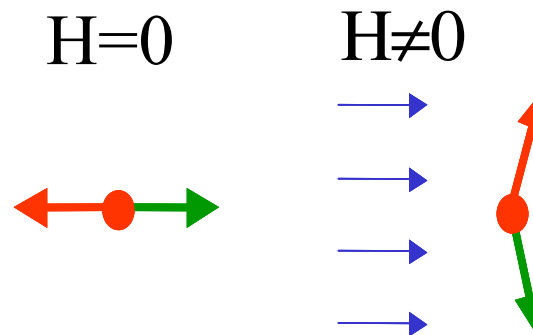


Free Layer Field Response

Conventional Free Layer





Tri-Layer Coupled Free layer



Single Domain Switching Model

- Balanced NiFe SAF free layer
- Write lines 45° to easy axis
- Unipolar currents, $\tau_p \approx 6$ ns

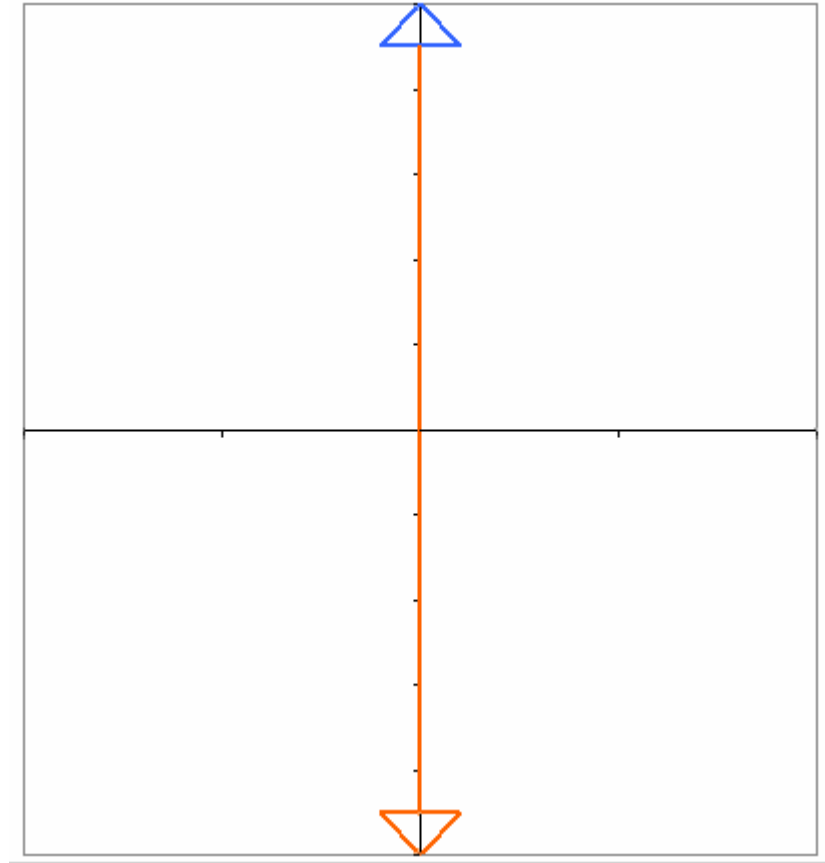
 = H

 = M


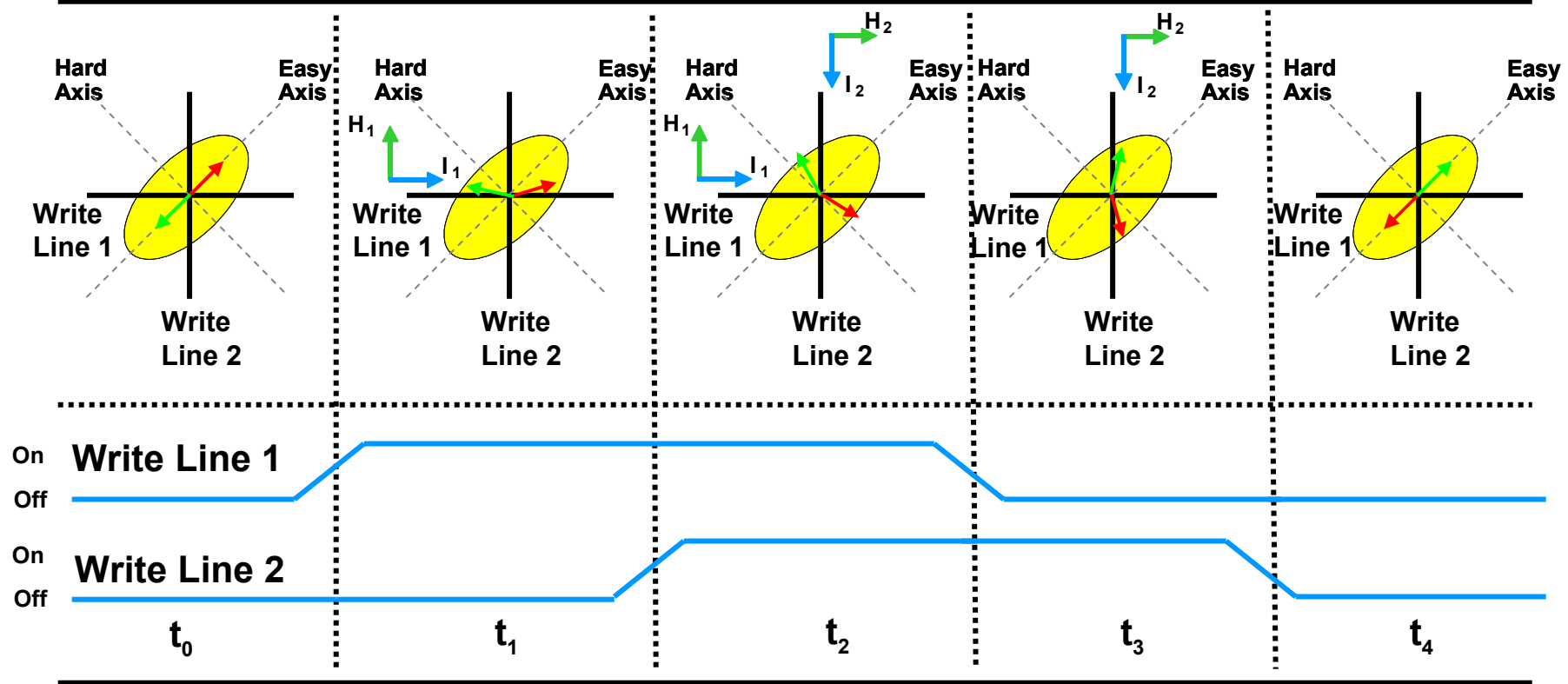
$$H_{sw}^{1,2} = \sqrt{\frac{H_k \cdot H_{sat}}{2}}$$

H_k = anisotropy field

H_{sat} = SAF saturation



Toggle MRAM Switching Sequence



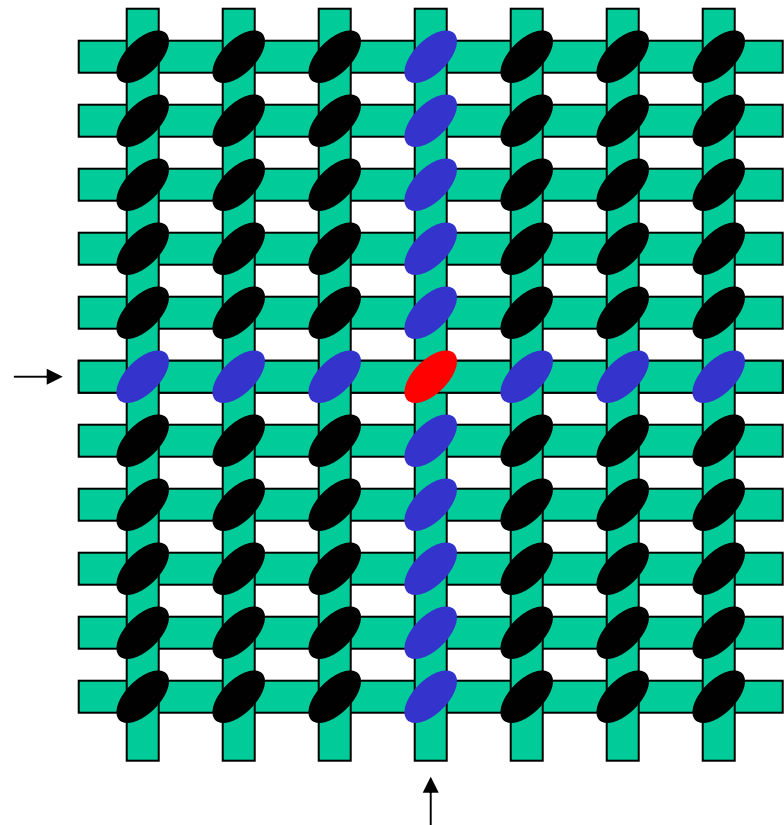
Unipolar currents

Overlapping pulse sequence

Pre-read / decision write

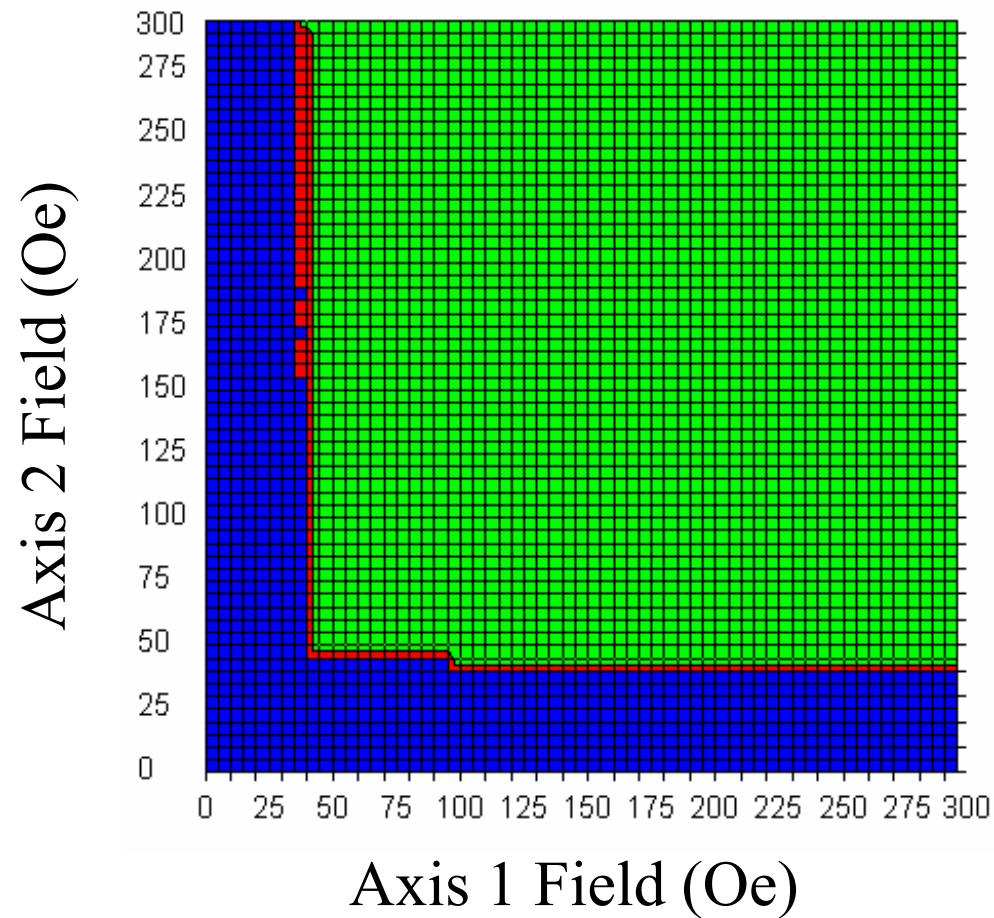
Toggle-Bit Selection

- High bit disturb margin
- All bits along $\frac{1}{2}$ -selected current lines have **increased** energy barrier during programming
- Requires overlapping pulse sequence for switching

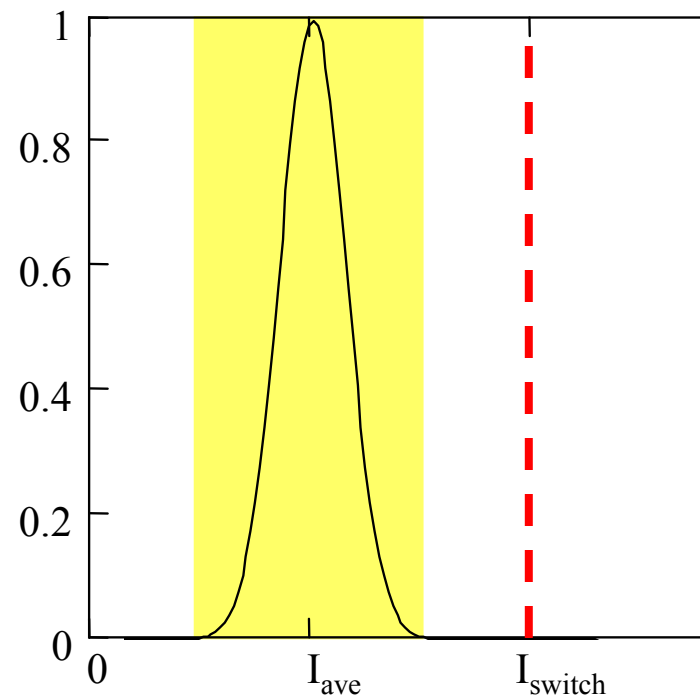
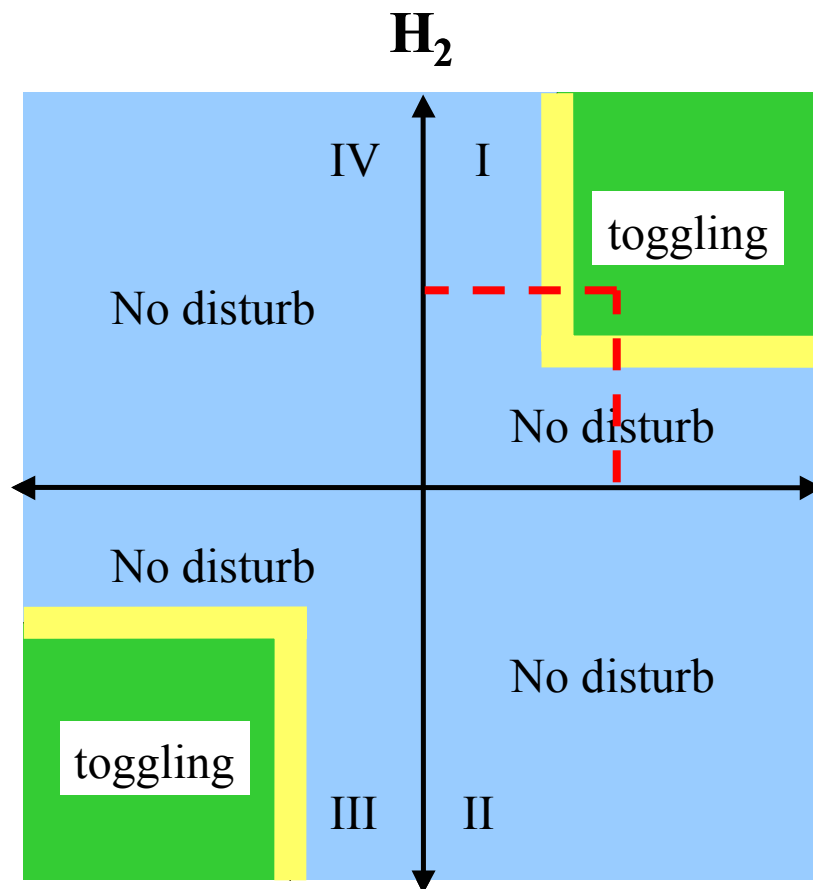


Measured Single Bit Switching

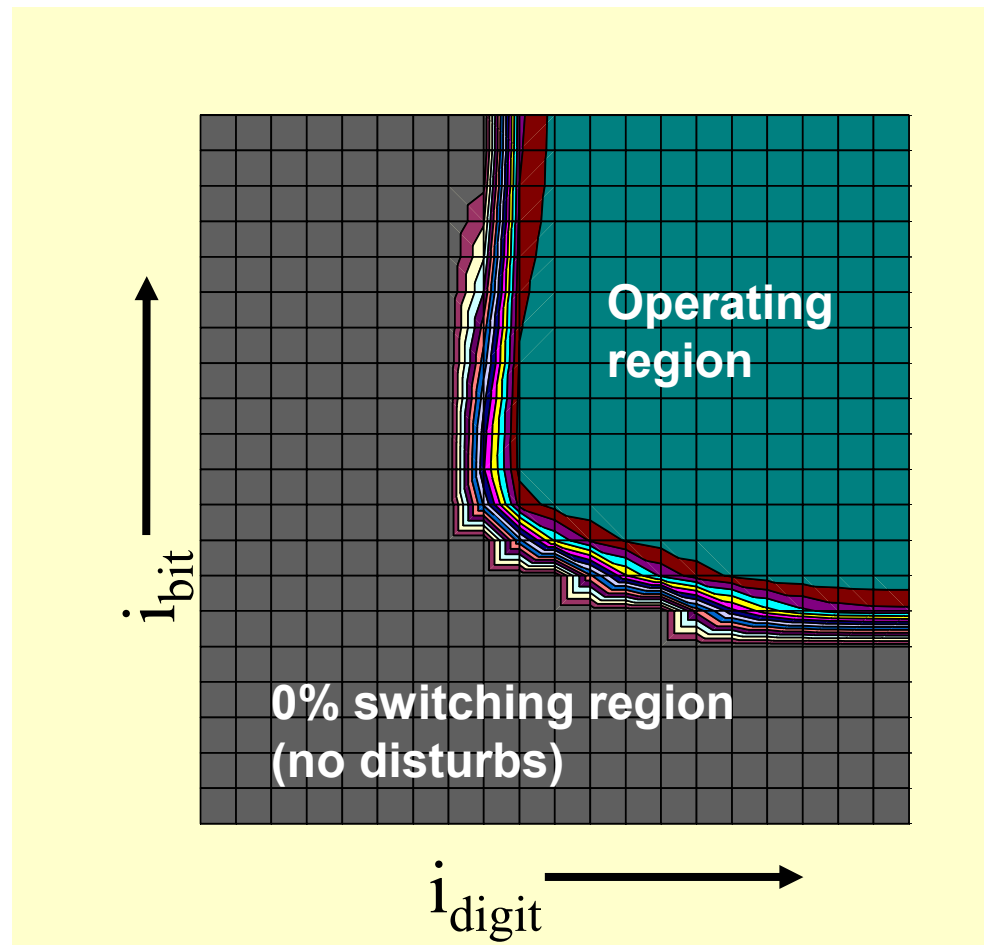
No disturb to > 300 Oe!



Toggle-Bit Array Characteristics



Measured Switching from 4Mb Toggle-MRAM



Opportunities in bit switching

The Savtchenko approach enables switching of bits with competitive sizes, within large arrays.

Innovations that would improve performance and assist in scaling to smaller dimensions include:

- **Fundamental understanding of switching dynamics and origin of switching distributions.**
- **Materials with high polarization and well-behaved permalloy-like magnetic properties**
- **Other devices that allow decreased switching current without thermal disturb**
- **Alternate switching approaches**
 - Is there something better than Savtchenko at smaller dimensions? (SMT?)
 - What are the engineering tradeoffs of the alternatives?

Summary

A 4Mb MRAM integrated into a 0.18 μ m CMOS process has been successfully demonstrated for the first time.

- MTJ optimized for read. Toggle writing scheme

Read: High quality, smooth, tunnel junctions are critical

- High MR is necessary but not sufficient
- Bit-to-bit resistance distributions and bias dependence of MR are critical
- Opportunities: higher polarization materials, improved tunnel barriers, band structure engineering?

Write: Toggle writing with balanced SAF enables current technology

- Improves: disturbs, operating window, data retention, scaling
- Opportunities: improved materials or alternate devices that can switch with less current, without sacrificing data retention, etc.

Photon-based methods

Materials Studies

- **Chemical and magnetic roughness, spin & orbital moments**
 - X-ray resonant magnetic scattering (XRMS)
 - X-ray magnetic circular dichroism (XMCD)
- **Best way to study interface sharpness, stability?**
- **Best test to prove or disprove $\frac{1}{2}$ metals?**

Magnetic Imaging

- **Domains, direction of moment in bits, element-specific studies**
 - Photoemission microscopy (PEEM)
 - Scanning transmission x-ray microscope (STXM)
- **Deep submicron resolution necessary to study micromagnetics of bit switching**
- **Time-resolved on the ns scale or below needed to observe bit switching**